Does Copper Pour on a Signal Layer Decrease Signal-to-signal Isolation?

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ANALOG HOME

Does putting a ground pour on PCB signal layers make the isolation better or worse? It can go either way, but with the proper knowledge and application, this technique will improve your designs.

In this article, I'll discuss how to simulate trace-to-trace isolation with true electromagnetic simulation software. We'll also cover a variety of rules of thumb that can help you stay away from trouble.

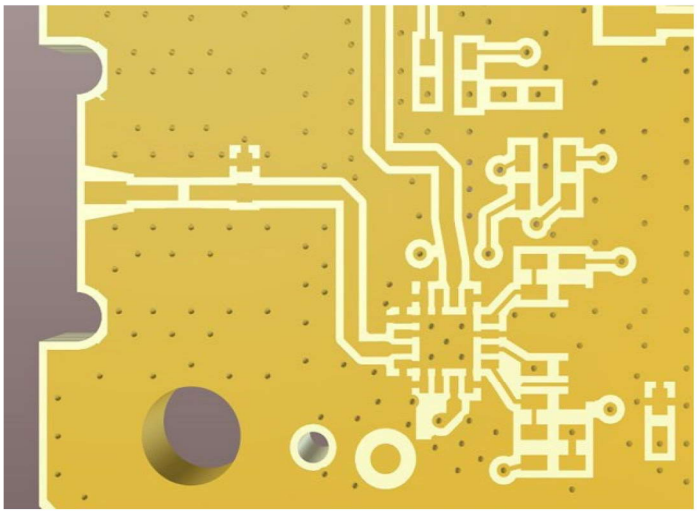

Figure 1: Many RF boards are built with CPWG construction because it offers much-improved EM performance. By improved, I mean smaller, less radiation, and better crosstalk performance than microstrip construction. This is essentially a copper pour on a signal layer and it works well, or legions of RF engineers would not be using it.

Fact or Fiction?

Recently an acquaintance told me, "I have heard that putting a copper pour on a signal layer between traces actually makes the isolation between the traces worse." I grabbed one of my RF boards (see Figure 1) and said, "If that is so, then how do all these RF boards that I have done with co-planar waveguide over ground manage to function? They all have copper pours on the signal layer, and they work to very high frequencies."[1]

Since co-planar waveguide over ground (CPWG), which is essentially "pouring copper on a signal layer," is used for a lot of RF work[2], and is proven to work for very high-performance RF circuits, how did this contradictory opinion catch on in the industry?

To investigate this, I used a one-inch section of 50-ohm microstrip consisting of an aggressor trace from ports 1 to 2 and a victim trace running in parallel from ports 3 to 4 as shown in Figure 2. I used typical values for the dimensions as might be on a real PCB. The trace width is 20 mils, with a spacing of 60 mils from

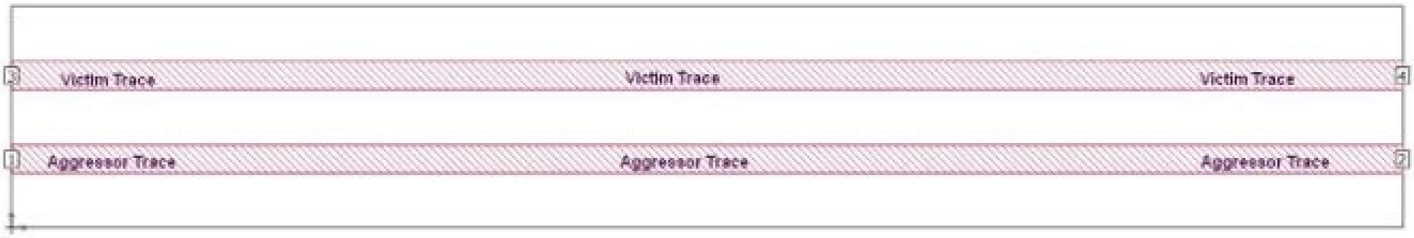

Figure 2: This 1-inch, 50-ohm aggressor trace (port 1 to 2) and victim trace (port 3 to 4) structure was modeled in Sonnet to study the effects of coupling between the traces.

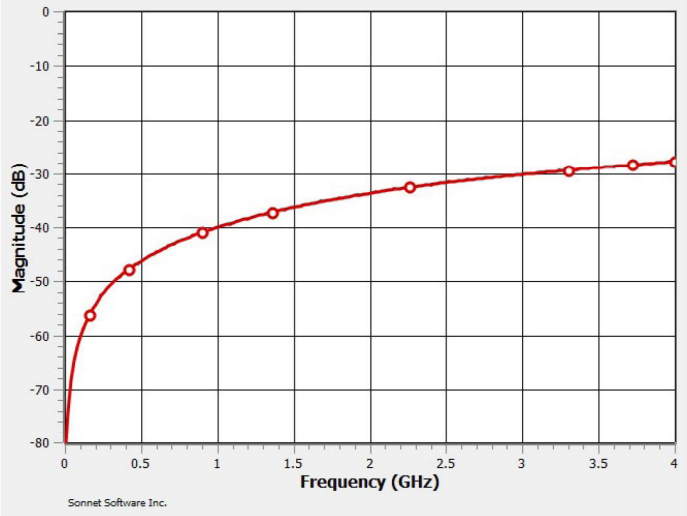

Figure 3: Simulating port 1 to port 4 coupling of the structure shown in Figure 2 shows nothing strange in the frequency range of 0-4 GHz.

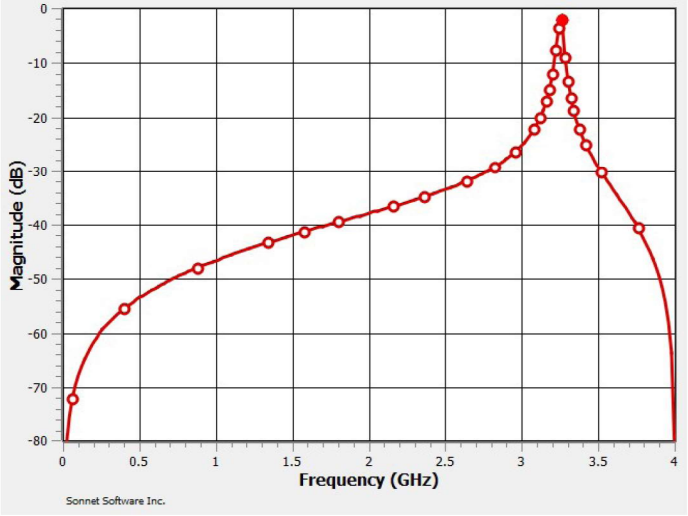

Figure 5: The resulting coupling measurement from ports 1 to 4 of the structure of Figure 3. This simulation does indeed show something strange going on at a frequency of around 3.2 GHz.

center to center, over an FR-4 substrate, 9.5 mils thick, with a modeled Er of 4.4.

When a Sonnet EM simulation[3] is run for the structure in Figure 2, and the coupling is measured from port 1 to port 4, as shown in Figure 3, you can see that there is nothing strange going on in the frequency range of 0-4 GHz. This is our baseline coupling that we will compare to later on.

Adding a copper pour to Figure 2 results in the new structure in Figure 4. The copper pour has a realistic spacing of 10 mils to the aggressor and victim traces and therefore has a minimal effect on the 50-ohm impedance of these traces.

Simulating the coupling of the traces and copper pour shown in Figure 4 results in the new coupling plot of Figure 5. The first response to seeing this is sure to be, "It's true. The isolation is worse with a copper pour." Perhaps, and perhaps not. It's all in understanding what is going on, because poorly placed copper will ruin any design, at any frequency from DC to light, as we shall see.

Antenna Basics

To understand what is going on with Figures 4, 5, and 6, we need to understand something about resonances and how antennas work. You may well have heard of a "half-wavelength" antenna. This is an antenna that is one-half of a wavelength long which has good efficiency as a radiator. There are also quarter-wavelength antennas, simply one-half of a half-wavelength antenna placed perpendicular to a perfectly conductive ground. Anything shorter will not radiate well at all without added matching.

If you put a trace or any copper structure

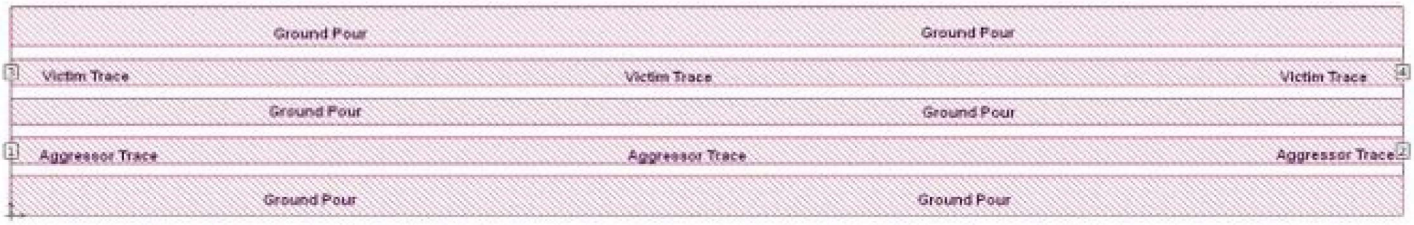

Figure 4: Adding a copper ground pour with a 10-mil gap to the aggressor and victim traces of Figure 2 results in this new structure.

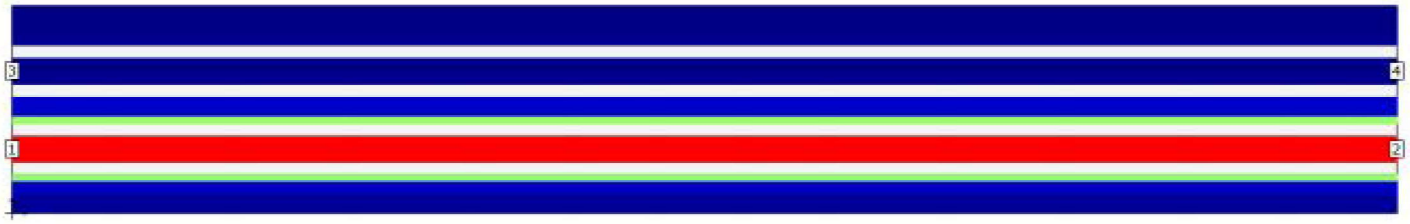

Figure 6a: It is interesting to look at the resulting current densities of the model in Figure 4 when excited. In this plot at 100 MHz there are no resonances present. As can be seen, all the high current is in the aggressor trace and along the edges of the copper pour as would be expected. Red is high-current density while blue is the lower-current density.

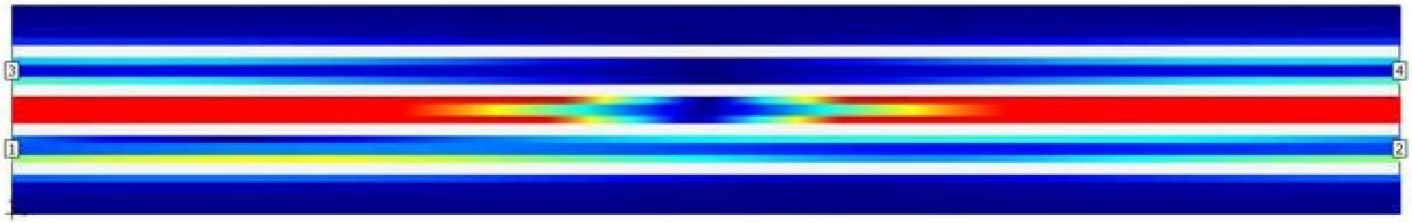

Figure 6b: At a frequency of 3.2 GHz, the resonance can clearly be seen. The victim trace has picked up a lot of current and that copper pour between the traces that we may have assumed was ground is anything but ground now. As can be seen, there is more current flowing in our pour than the signal traces themselves! Red is high-current density while blue is the lower-current density.

on a PCB that is a quarter or half or multiples of a quarter wavelength, they too can be resonant and exhibit very good radiation at specific frequencies, and at every quarter wavelength above that: half, three-quarters, full wavelength, etc.

This is what we see in Figures 4, 5, and 6. We may have assumed that the copper pours are ground, and they are at DC and low frequencies. However, at a sufficiently high frequency, they will resonate as has been shown in Figures 5 and 6. What we have unwittingly made with the structure of Figure 3 is an edge-coupled bandpass filter[4], not a trace shield.

Rules of Thumb

A common rule of thumb is that a signal propagates on a typical FR-4 type PCB at about half the speed of free space[5]. Hence a wavelength at a given frequency is given as Equation 1.

Equation 1

$$\lambda = \frac{Vp}{f} \text{ or } \frac{6.4\,ns/inch}{f\,GHz} = \lambda \text{ inches}$$

Where λ is the full wavelength in inches. Rearranging the equation above to give us the critical, quarter wavelength frequency terms of frequency and length results in Equation 2.

Equation 2

$$1/4\,Wave\,Length \text{ inches} = \frac{1.6\,nS/Inch}{f\,GHz}$$

And re-arranging again, as a function of length,

Equation 3

$$f \text{ GHz} = \frac{1.6\,nS/Inch}{1/4\,Wave\,Length \text{ inches}}$$

For example, knowing that the copper pours in Figure 4 are 1 inch long, Equation 2 predicts that the quarter wavelength frequency is 1.6/1 = 1.6 GHz and the half wavelength is 3.2 GHz, which is exactly where we see the peak resonance of our Sonnet simulation in Figure 5.

The upper equation above can predict the critical trace length based on the frequency of operation. For example, if a trace is carrying a

100 MHz SPI clock, we know that the rule of thumb is that a square wave needs at least five harmonics to accurately reproduce the square wave shape. The quarter wavelength length would then be approximately: 1.6/0.5 = 3.2 inches. Any trace less than about 3.2 inches carrying this clock will have poor efficiency as a radiator.

Another common rule of thumb is if you don't have a repetitive clock signal but instead have a fast rise-time signal. The bandwidth of a known rise-time is shown in Equation 4.

Equation 4

$$f\ \text{GHz} = \frac{0.35}{Tr\ \text{nSec}}$$

Where Tr is the rise time of the pulse in nanoseconds and f is the equivalent bandwidth of the signal in GHz. It is well known that a 1 ns rise time is approximately equivalent to a 0.35 GHz (or 350 MHz) signal bandwidth.

Given these rules of thumb, we can calculate the critical trace lengths in terms of frequency and rise time of our signals. Normally all our logic edges are quite fast now, faster than they need to be for most clock signals, so I normally use the rise-time equation to figure the required bandwidth and then use that to calculate the critical trace lengths to watch out for.

This "less than a quarter wavelength" rule of thumb applies to all sorts of analysis situations and is a useful thing to keep in mind during the design, and perhaps more importantly, troubleshooting of higher-frequency PCBs[6].

The Fix

Now that we understand what the critical frequencies and lengths are we can move on with our simulations and solutions.

We have just proven that any copper structure, trace, pour, or ground plane can and will act as a resonant antenna if its length gets to or exceeds a quarter or half wavelength of the excitation frequency.

Now, look back to the very first picture of a CPWG layout in Figure 1. Notice anything in those copper pours? Can you see the little vias all along the periphery of the copper pours? I didn't put those there just because I wanted to make life miserable for my PCB fabricator. Actually, those vias stitch the grounds together and effectively provide a way to shorten the length of the copper pours to be less than a quarter wavelength.

How can we fix Figure 4 then? How about effectively making the copper pour in Figure 4 smaller in any direction less than a quarter wavelength? If we place ground stitching vias in the copper pours we can achieve this, as shown in Figure 7.

The addition of properly spaced stitching vias in the copper pour shows that at any frequency, now, the central copper pour acts like a ground and never gets hot as it did in Figures 5 and 6, even at the highest frequency of this sweep (Figure 8).

When properly done, copper pour is indeed acting as the true shielding ground plane that we had envisioned it would be when we put

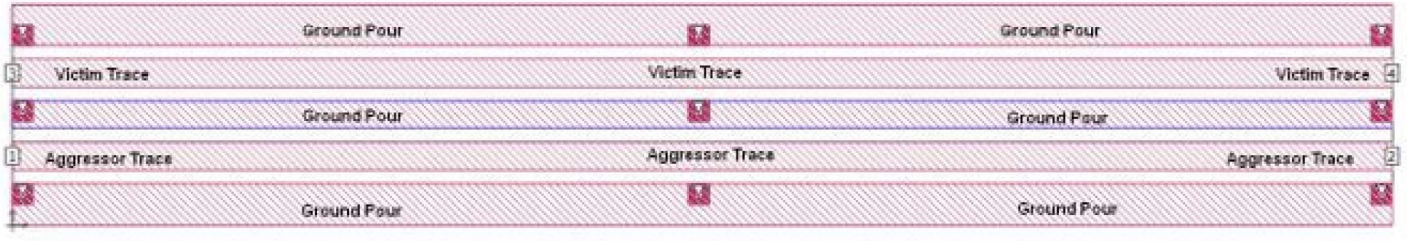

Figure 7: To fix that hot central copper pour we can apply stitching vias to the ground return layer and effectively make the copper pours appear electrically shorter at high frequencies and make them appear more like the ground they were supposed to be in the first place. Here I placed the vias (dark red squares) symmetrically at a distance of 0.5 inches to divide the central copper pour into sections less than the quarter wavelength at 3.2 GHz.

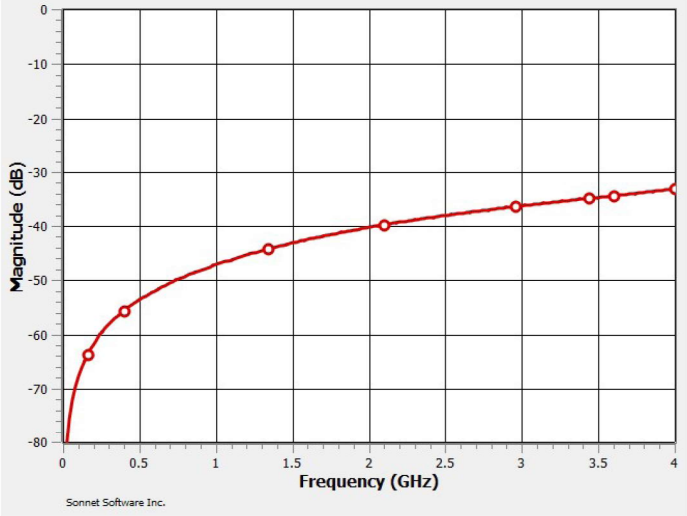

Figure 8: Simulating our structure of Figure 7 with the addition of stitching vias placed in the copper pours shows the resonances are now completely gone.

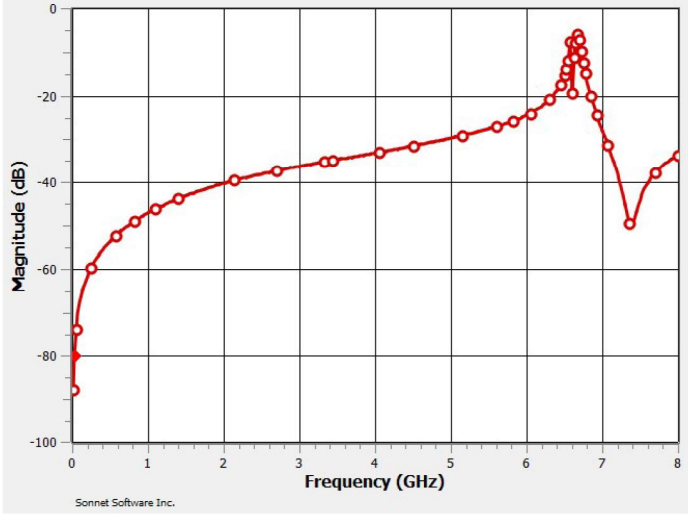

Figure 10: Now, it is predicted that the properly stitched copper pours of Figure 7 will have a new resonance peak at around 6 GHz and that is exactly what we find. We can either place the stitching vias closer together or know that these simulations are done with lossless materials and any real FR-4 PCB will start to have significant losses above 3 GHz, which will be much less of an energetic peak than simulated here.

it there, and it is not making the isolation from the aggressor to the victim trace worse. Comparing the isolation curve of the original model simulation (Figure 3) with our properly stitched ground pour (Figure 8) shows that the added isolation of adding a properly grounded copper pour is about 8 dB in this simulation as shown in Figure 9. Certainly, to me, adding properly done copper pours to all my layers is worth doing for the improved isolation and the improved EM radiation performance of the PCB.

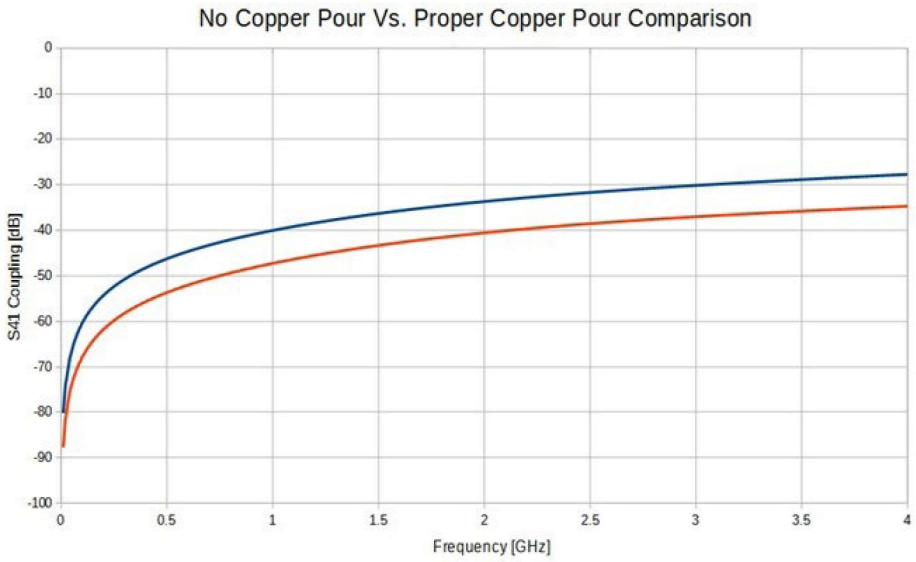

Figure 9: Comparing the isolation curve of the original model simulation (blue curve) with our stitched ground pour (orange curve) shows that the added isolation of adding a properly grounded copper pour is about 8 dB in this simulation as shown. This is proof that properly done, adding ground pours to signal layers does indeed improve signal-to-signal isolation.

You might now ask: "Since the stitching vias are at 0.5 inch spacing in this example, won't there be a new resonance at 6 GHz now?" And you would be right; extending the sweep frequency of the structure of Figure 7 up to 8 GHz does indeed show a new resonance at 6 GHz, just as we predicted (Figure 10).

We can continue pushing the undesired resonance frequency up by decreasing the space between the stitching vias, and this is one of the reasons I use the less than quarter wavelength as the rule of thumb on spacing in the first place, as it gives plenty of

margin in the final design. Remember also that these simulations are modeled with lossless copper and substrate material. Any real FR-4 PCB will start to have significant losses by 3 GHz, and these losses always help by lowering the peak currents and undesired coupling at very high frequencies.

Application

As we have seen, every copper structure on the PCB must be less than a half a wavelength, and preferably less than a quarter wavelength, for the highest frequency at which the structures will be excited[6].

Here is how I apply the "less than a quarter wavelength" rule of thumb when I start laying out a PCB. I calculate what a quarter wavelength is for the highest frequency signal on my PCB, and I make a note of that. If I strategically place my vias at a distance less than this around my high-frequency copper pours I will be fine, and there will be some places where I can't maintain this spacing because of other routing requirements, and that's okay. In those places, you can skip one of the vias or place them as best you can at slightly larger distances and the PCB will still work. You can see this in Figure 11 where some vias appear missing because I had to dodge other traces on other layers; your design will still work.

You probably can't tell your PCB software tool that there is a constraint of a via every "X inches," but at the end of the design, you can set the visible grid to whatever you calculated as the appropriate spacing and make sure that the grid is displayed and very bright. This will give you visual cues as to how you did placing the vias and where you may need to squeeze in more.

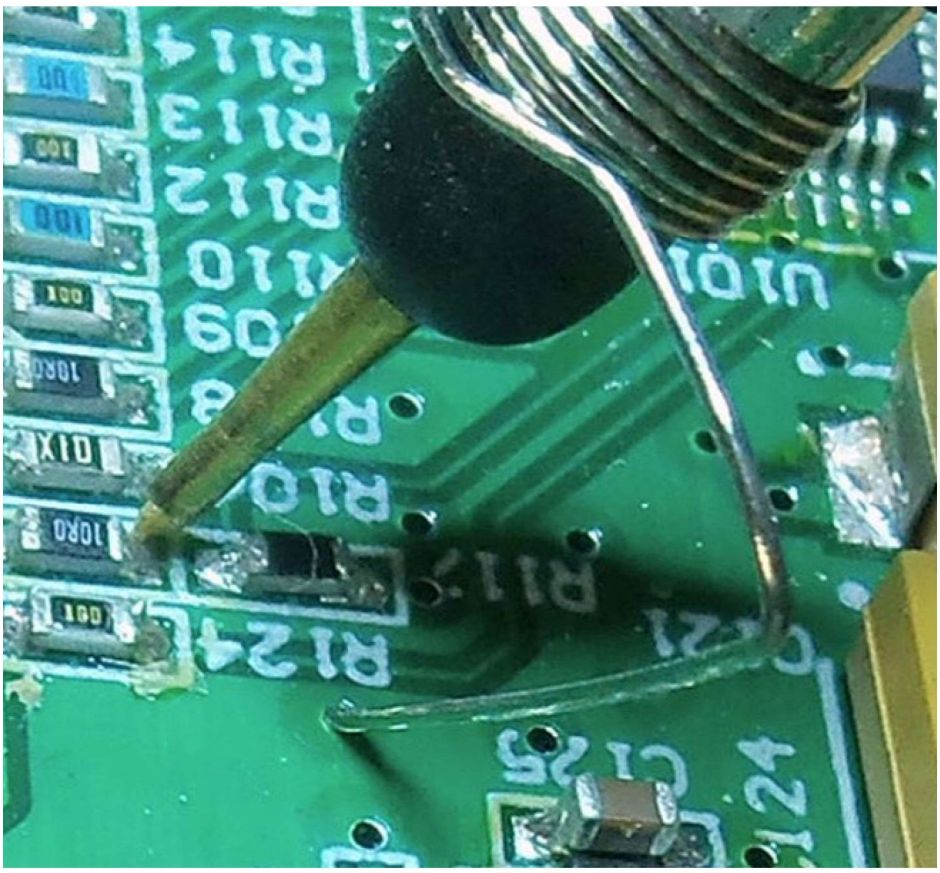

Figure 11: Having a ground pour on the outer signal layers helps when probing high-frequency signals; it is quite easy to place the scope probe ground spring into a nearby stitching via to make the ground contact. Even "slapping on" resistors and capacitors to fix design issues is easier when you have copper pours on the outer layers, and honestly: Who hasn't had to add a part to fix a prototype now and again?

A final note on stitching via hole sizes: If you look at some of the pictures of evaluation boards on the internet[2], you will see that a lot of the time very large holes are used for the stitching vias. This is because, in an X/Y view from the plane of the PCB traces, a large hole has a large copper width in the X and Y directions of the PCB.

This large hole effectively makes a wall-like structure, instead of the "stake" that a smaller hole would produce, and it makes the stitching more effective at higher frequencies with a smaller number of drill holes needed. While using a large hole has advantages on a simple evaluation board, these large holes also block the routing channels needed for more complex PCBs. I usually use my design's minimum hole size for my stitching vias to keep my routing options open, and it works just fine.

Other Benefits

There are other benefits to having a convenient ground on the outside signal layers.

- **Scope probing:** Having ground available helps when probing with an oscilloscope as shown in Figure 11. This is especially true when probing any clock signal where you simply cannot use the long flying lead of the scope probe.
- **Fixing errors:** Well, who hasn't designed a circuit that needed a resistor or capacitor "slapped" onto it to get it to work properly? Having a ground nearby on the top and bottom layers makes this trivially easy.
- **Improved radiation performance:** A properly placed copper pour on the signal layers does indeed reduce the radiation of the design in general by bending the electric field lines into the copper pour and not letting them be so far out into space. Think about it this way: If I create an antenna trace on a PCB and then I surround it with copper pours on just the sides, I will have made a sort of coaxial structure, and I have ruined that trace's effectiveness as a radiator because I have shorted out the electric field from the surrounding air. Everyone can probably reason that a coax cable is the best way to transfer signals without radiation, right? A properly designed copper pour does nearly the same thing to nearby traces. Note that you may have to adjust the final trace width to maintain the desired impedance levels with a close copper pour[7].
- **Heatsinking:** More copper means better heat sinking in general for the PCB as a whole, and the stitching vias thermally tie it all together.

Possible Downsides of Adding Copper Pours

There may also be disadvantages to this approach.

- The possible increased cost of adding vias and then having to drill them
- Takes time to add copper pours and the stitching vias correctly
- Incorrectly done copper pours may indeed make the situation worse

Conclusion

It isn't a matter of, "Copper pours on a signal layer make things worse." It's more like, "Poorly placed copper anywhere will ruin any design." Once you understand what is really going on, with the help of easy-to-use EM simulation tools, you will improve your designs immensely. DESIGN007

References

1. "How to Make a Quick Turn PCB That Modern RF Parts Will Actually Fit On," and "Benefits of Coplanar Waveguide Over Ground," by Steve Hageman.
2. For more examples of boards created with CPWG construction, just do a web image search for "Hittite Evaluation Board." Hittite (now part of Analog Devices) is famous for doing all their prototype boards using the CPWG technique.
3. The Sonnet EM simulator and a free lite version are available at www.sonnetsoftware.com.
4. To see examples of filters of this type, do an internet image search for edge-coupled filters.
5. "Propagation Times and Critical Length—How They Interrelate," by Douglas Brooks.
6. Another example of using the "quarter of a wavelength" rule of thumb, visit AnalogHome: Decoupling RF Circuits - Part 1.
7. There are numerous free calculators available that will do calculations for CPWG structures, or you can use Sonnet.

Steve Hageman is the founder and lead engineer at Analog Home.